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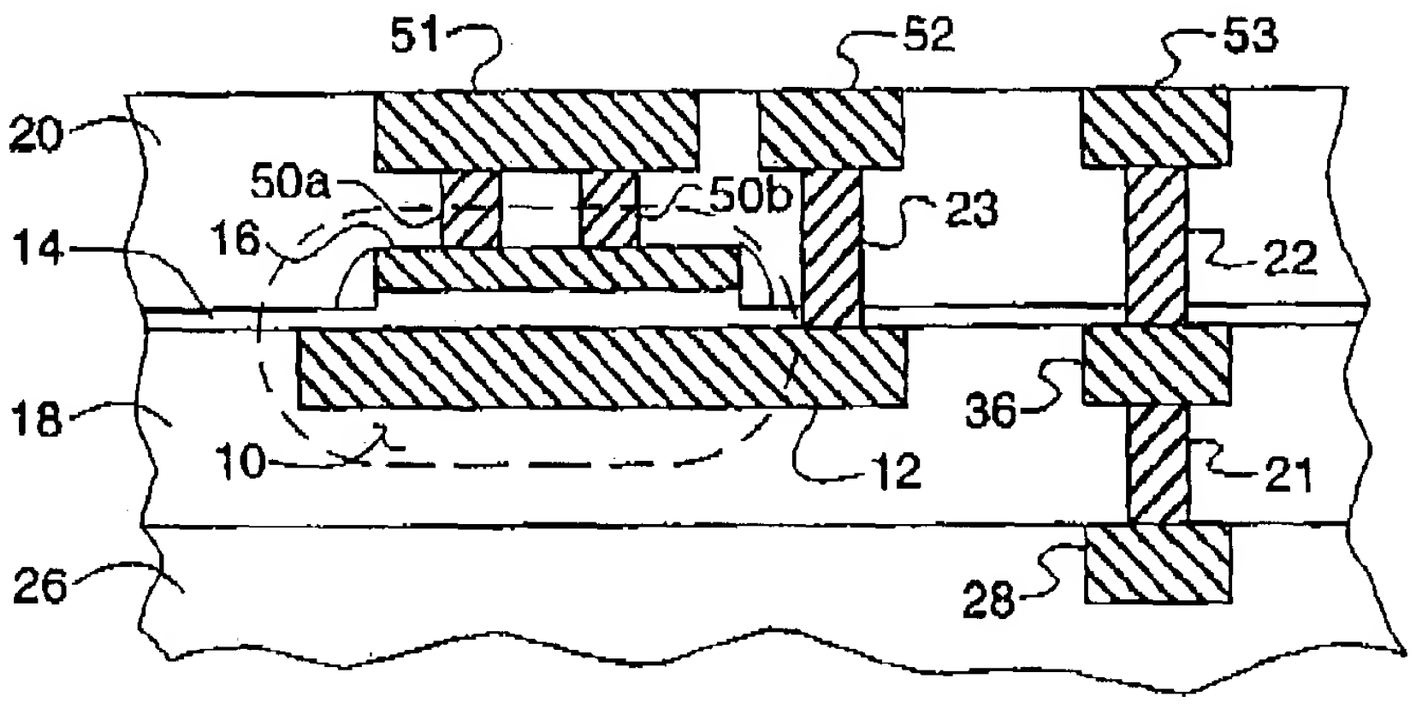

(57) Abstract

An improved thin-film capacitor and methods for forming the same on a surface of a substrate are disclosed. The capacitor includes a bottom conducting plate formed by depositing conductive material within a trench of an insulating layer and planarizing the conducting and insulating layers. A dielectric film is then deposited on the substrate surface, such that at least a portion of the dielectric material remains over the bottom conducting plate. A second conductive layer is then deposited over the surface of the substrate, patterned and etched such that at least a portion of the second conducting material resides over at least a portion of the dielectric material.

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THIN-FILM CAPACITORS AND METHODS FOR FORMING THE SAME

FIELD OF THE INVENTION

The present invention relates generally to capacitors in microelectronic devices. More particularly, the present invention relates thin-film capacitors and methods for forming the same.

BACKGROUND OF THE INVENTION

Formation of predictable, reliable capacitors may be desirable for several reasons. For example, mixed signal, radio frequency, and other circuits or devices may desirably include integrated capacitors with predictable and reliable electrical characteristics. In particular, these devices preferably include capacitors with low voltage coefficients (change of capacitance with voltage over an operating range), good capacitor matching, and relatively predictable capacitor values. In addition, if capacitors form part of an integrated circuit, it may be desirable to minimize additional processes or changes to processes required to form the capacitor. Accordingly, it is often desirable to form such capacitors using substantially standard semiconductor process flows such as CMOS, bipolar, and BiCMOS processes.

Capacitors for microelectronic devices and the like may be formed in a variety of configurations. Often, such capacitors include two substantially parallel layers of conductive material separated by an insulating layer. Conductive materials typically include doped silicon substrate, polysilicon, or metal; insulating materials typically include a dielectric material such as silicon oxide, silicon nitride, silicon oxynitride, tantalum oxide, barium strontium titanate, or other insulating materials.

The thin-film capacitor is generally formed by depositing, patterning, and etching various layers on a substrate. Typically, a first parallel layer of conductive material (a base plate) is formed by depositing the conductive material over the surface of the substrate, wherein the substrate may be a semiconductor wafer with several layers of conducting, insulating, semiconducting and semi-insulating layers thereon.

Alternatively, the conductive material may be formed by doping the semiconductor substrate with substantially conductive material.

If the base plate is formed by depositing conductive material on the wafer surface, the material may be patterned with photoresist and etched using an appropriate wet or dry etch process. Similarly, and regardless of how the base plate was formed, the insulating layer may be formed by depositing insulating material over the surface of the wafer, patterning the insulating material, and etching the insulating material leaving at least some insulating material over at least a portion of the conducting layer. A second conducting layer (top plate of the capacitor) may be formed over the insulating layer in a like manner.

Typical capacitor materials and configurations of top and base capacitor plates generally include: a polysilicon top plate and a doped substrate base plate, a polysilicon top plate and a polysilicon base plate, metal top plate and a polysilicon base plate, and metal top plate and a metal base plate. Of these various capacitor configurations, the metal to metal capacitors may be particularly advantageous because, among other reasons, they allow for increased distance from the substrate to the bottom plate, and they generally have lower voltage coefficients due to reduced voltage induced depletion effects at the metal to dielectric interface.

In an effort to reduce device and circuit costs, it is generally preferred to reduce the size of the devices and circuits and their corresponding capacitors. Capacitor size, for a given capacitance, may be reduced by increasing the capacitor's capacitance density. The increase in capacitance density can be achieved by using insulating layers with higher dielectric constant, by reducing the thickness of the insulating layer, or a combination thereof.

The preferred distance between conducting layers for a given dielectric material is often governed by voltage breakdown design parameters, and the breakdown voltage parameters are generally dependent upon, among other things, the minimum distance between conducting layers. If either the insulating layer or the conducting layers, or a combination thereof have rough surfaces, the insulating layer thickness may have to be increased to compensate for the thinner regions of the layer such that the thinnest portion of the insulating layer provides adequate (*e.g.*, sufficiently high) breakdown voltage characteristics.

One method of smoothing a surface of the insulating or conducting layer is to use chemical mechanical planarization (CMP). A capacitor formed by using CMP to form the top and bottom plates of a capacitor is disclosed in United States Patent Number 5,708,559, issued to Brabazon et al. on January 13, 1998. The '559 patent discloses methods of forming a capacitor on a surface of a wafer by forming a trench in an insulation layer, depositing metal over the insulation layer and planarizing the surface of the wafer to form the bottom plate of the capacitor. A thin layer dielectric is then deposited and patterned over the first capacitor plate, and this layer is patterned and etched such that a portion of the first metal plate of the capacitor is exposed. A second insulator is then deposited on the wafer surface and openings are etched into the second insulating material. A second metal layer is then deposited on top of the insulating layer, filling the openings, thereby forming a contact to the first and second plates of the capacitor.

While the '559 patent discloses methods for forming thin-film, metal-insulator-metal capacitors on a surface of a wafer, the disclosed processes generally include either excess or additional photoresist masking steps to form the capacitor plates, which may increase overall wafer fabrication costs, or the methods include etch stops on a part of the dielectric that communicates with the top capacitor plate. Use of such etch stops may cause variation of capacitance values due to capacitor formation processing and the like. In addition, the disclosed methods generally require etching through thick insulating layers to define the capacitor plate. Etching of these thick layers typically results in increased variation of the trench dimensions that define the plate dimensions. This variation may in turn cause variation in the electrical properties of the capacitor. In addition, the processes disclosed in the '559 patent may include additional processing steps to form electrical contacts to the bottom metal plate capacitor. Simplified, cost-effective, and well defined capacitor flows that may allow capacitor formation in multiple levels of metallization are therefore desirable.

Therefore, a need exists for improved thin-film capacitors and for methods of forming the capacitors.

SUMMARY OF THE INVENTION

The present invention provides improved thin-film capacitors and methods for forming the same. While the way in which the present invention addresses the various

disadvantages of presently known capacitors will be addr ssed hereinbelow, in general, the invention provides a capacitor that is reliable. In addition, the capacitor of the present invention may be formed with minimal additional processing steps.

In accordance with a preferred embodiment, a spacer is formed around a capacitor plate to reduce damage to the plate due to subsequent processing steps.

In accordance with another preferred embodiment of the present invention, portions of the capacitor are formed concurrently with other device features.

In accordance with another preferred embodiment of the present invention, a capacitor plate is formed by forming a trench in a first insulating material. Conducting material is then deposited over the surface of the wafer, filling the trench. The conducting material is then planarized to produce a plate of the capacitor within the trench. A second insulating material is then deposited over the surface of the wafer to form the capacitor dielectric. Next, the top plate of the capacitor is formed by depositing conducting material over the surface of the wafer and patterning and etching the conducting material to form the top plate and define the capacitor area.

In accordance with a further preferred embodiment of the present invention the capacitor dielectric overhangs the base plat. The top plate of the capacitor is formed by depositing conductive material over the surface of the wafer and patterning and etching this layer to form the top plate, define the capacitor area, and provide electrical connections to the top plate, the bottom plate, or combinations thereof.

In accordance with another preferred embodiment of the present invention, a capacitor plate and conductive plugs are formed in a first insulating material. The capacitor and conductive plugs are formed by depositing conductive material over a surface including trenches and vias. The conductive material is then planarized to produce the base plate of the capacitor in the trenches and conductive plugs in the vias. A second insulating material, the capacitor dielectric, is then deposited over the surface of the wafer. Next, the top plate of the capacitor is formed by depositing conductive material over the surface of the wafer and patterning and etching this layer to form the capacitor top plate, define the capacitor area, and provide electrical connections to other portions of the wafer. Another dielectric thin film is then deposited and then etched back to form a sidewall spacer along the perimeter of the capacitor top plate to protect the capacitor perimeter during potential interaction from

subsequent processing steps. Other films such as insulating materials may then deposited as an interlevel dielectric to the next conductive layer. Accordingly, a via may be formed within the interlevel dielectric material and conductive plugs may be formed therein to provide electrical connections to the capacitor.

In accordance with a further preferred embodiment of the present invention, the top plate may overhang the base plate of the capacitor. This may allow etch steps which are less selective between the top conductive layer and various insulating materials to be used during capacitor formation.

In accordance with a further preferred embodiment of the present invention, the top plate of the capacitor may be offset from the base plate of the capacitor. This allow various electrical connections to the top and base plates to be made from either the top or bottom of the respective plate.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the drawing figures, wherein like reference numbers refer to similar elements throughout the figures, and:

Figure 1 is a schematic cross-sectional diagram of a semiconductor wafer including a thin-film capacitor in accordance with the present invention;

Figure 2 is a schematic cross-sectional diagram of a wafer showing trenches and vias formed within an insulating layer;

Figure 3 is a schematic cross-sectional diagram of the wafer shown in Figure 2 with conductive material deposited over the surface of the wafer;

Figure 4 is a schematic cross-sectional diagram of the wafer shown in Figure 3 after the conductive material has been removed from a portion of the wafer surface;

Figure 5 is a schematic cross-sectional representation of the wafer shown in Figure 4 with a dielectric film and a conductive material deposited on the wafer surface;

Figure 6 is a schematic cross-sectional diagram of the wafer shown in Figure 5 with a top plate of a capacitor formed on the surface of the wafer;

Figure 7 is a schematic cross-sectional diagram of the wafer shown in Figure 6 with a second dielectric film deposited on top of the wafer;

Figure 8 is schematic cross-sectional diagram of the wafer shown in Figure 7 with the second dielectric film etched back to form sidewall spacers along the perimeter of the capacitor;

Figure 9 is a schematic cross-sectional diagram of a thin-film capacitor on a surface of a semiconductor wafer in accordance with an alternate embodiment of the present invention;

Figure 10 is a schematic cross-sectional diagram of a wafer including a capacitor formed at an interior portion of the wafer in accordance with an alternate embodiment of the present invention;

Figure 11 is a schematic cross-sectional diagram of a wafer including a thin-film capacitor formed thereon in accordance with an alternate embodiment of the present invention;

Figure 12 is a schematic cross-sectional diagram of a wafer including a thin-film capacitor having a top plate overhanging a bottom plate in accordance with an alternate embodiment of the present invention;

Figure 13 is a schematic cross-sectional diagram of a wafer including a thin-film capacitor in accordance with an alternate embodiment of the present invention;

Figure 14 is a schematic cross-sectional diagram of a wafer including a thin-film capacitor in accordance with an alternate embodiment of the present invention;

Figure 15 is a schematic cross-sectional diagram of a wafer including a thin-film capacitor including an etch stop in accordance with an alternate embodiment of the present invention;

Figure 16 is a schematic cross-sectional diagram of a wafer showing an etch stop layer and a via formed therein;

Figure 17 is a schematic cross-sectional diagram of the wafer of Figure 16 with an insulating layer and trenches formed therein;

Figure 18 is a schematic cross-sectional diagram of the wafer of Figure 17 with a capacitor plate formed within a trench;

Figure 19 is a schematic cross-sectional diagram of the wafer of Figure 18 with an etch stop layer over the plate; and

Figure 20 is a schematic cross-sectional diagram of the wafer of Figure 19 with a capacitor top plate formed thereon.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention generally relates to capacitors formed on a substrate surface and to methods for forming the capacitors. More particularly, the invention relates to forming thin-film capacitors on a substrate surface using chemical mechanical planarization (CMP). While the thin-film capacitors of the present invention may be formed on the surface of any substrate, the present invention is conveniently described in connection with the surface of a semiconductor wafer, wherein the wafer may have several layers of conducting, insulating, semi-conducting and semi-insulating layers deposited and patterned thereon. Further, during formation of the capacitor or other microelectronic devices on a semiconductor surface, the surface of the wafer may change from step to step in the fabrication process. Therefore, as used below, the term surface generally means the top of the semiconductor wafer, and may not necessarily refer to any particular film or device structure.

A thin-film capacitor 10 in accordance with the present invention is shown in Figure 1. Thin-film capacitor 10 generally includes a base plate 12, a dielectric layer 14 and a top plate 16. Thin-film capacitor 10 is typically surrounded by insulating layers 18 and 20, and electrical plugs 22 are typically used to form electrical contacts to various components on the wafer.

In accordance with various embodiments of the present invention, methods of forming capacitor 10 and other features on the wafer preferably require few additional steps (*e.g.*, deposition, masking, and etching steps) that are specific to capacitor 10 formation. In addition, preferable embodiments are generally configured such that capacitor 10 may be formed at various metallization levels. Accordingly, the preferred capacitors and methods described below are designed to be substantially robust such that they may be formed or implemented at various metallization levels on the wafer surface.

With reference to Figures 2-8, thin-film capacitor 10 may be formed on a surface 24 of a semiconductor wafer. Surface 24 may include any material and preferably includes an insulating film 26 and a conductive feature 28. Insulating film 26 may include any material that is resistant to the conduction of electricity. Such materials may include doped or undoped silicon oxide, phosphosilicate glass, tetraethylorthosilane (undoped or doped with boron and/or phosphorous), low-k

dielectric materials such as spin on dielectrics, fluorinated oxides, or the like. Conducting feature 28 may include any material capable of conducting electricity such as, for example, polysilicon, doped polysilicon, tungsten, aluminum, copper, titanium nitride, any combination thereof, or the like.

In preferred aspects of this embodiment of the present invention, base plate 12 is generally formed within insulating layer 18 using damascene processing, which includes forming a trench or the like, filling the trench with material, and removing any excess material from the surface. Accordingly, capacitor 10 formation generally begins with depositing insulating layer 18 onto surface 24 of the wafer. Insulating material 18 may include any material that is resistant to conduction of electricity. Preferably, insulating material 18 includes an oxide, a doped oxide, a low-k dielectric material, any combinations thereof, or the like. For example, insulating material 18 may include silicon oxide. Insulating material 18 is preferably planarized using CMP to provide a smooth surface for subsequent processing. As discussed in greater detail hereinbelow, planarizing a surface may facilitate relatively precise transfer of a pattern onto a surface.

Referring now to Figure 2, insulating layer 18 may be patterned and etched to form trenches 30, 32 and a via 34. Trenches 30, 32 and via 34 may be formed by any methods now known in the art or hereafter devised. For example, trenches 30, 32 may be formed by patterning the surface of material 18 with an etch-resistant substance and exposing portions of material 18 to an etchant. In accordance with various aspects of the present invention, trenches 30, 32 and via 34 may be formed with the same or distinct masking and etching steps; however, trenches 30, 32 and via 34 are preferably formed during separate steps.

Referring particularly to Figure 3, base plate 12 of capacitor 10 and a conductive line 36 may be formed by depositing a conducting material 38 over the surface of insulating layer 18. Conducting material 38 may include any material that allows conduction of electricity. In preferred embodiments of the present invention, conducting materials may include metals such as copper, tungsten, aluminum, or titanium nitride. In particularly preferred embodiments of the present invention, conducting material 38 includes a barrier metal of about 0 to about 800 Å of titanium

nitride, titanium, tantalum, tantalum nitride, combinations thereof, or the like and about 1000 to about 10000 Å of copper, aluminum, or tungsten.

In accordance with a preferred aspect of this embodiment, base plate 12 may be conditioned to prevent dielectric layer-conducting layer interface degradation. Conditioning techniques may include a sputter clean, passivation anneals in atmospheres of oxygen, nitrogen, hydrogen, other gases, and combinations thereof. In addition, a thin barrier layer (not shown) having a thickness of about 50 to about 500 Å may be deposited onto surface 40. In this case, additional masking and etching steps may consequently be necessary to remove the barrier layer from material 18 surface to prevent shorts between the base plate 12 and feature 36 and the like.

Referring now to Figure 4, base plate 12 and feature 36 are defined by removing a portion of conducting material 38 such that the top of conducting material 38 is substantially in the same plane as the top of insulating layer 18. Preferably, the portion of conducting material 38 is removed using CMP. Using CMP to remove a portion of conducting material 38 is advantageous for capacitor formation because, among other reasons, it provides a smooth top surface 40 of base plate 12 for improved capacitor 10 performance.

Referring now to Figure 5, dielectric layer 14 of capacitor 10 may be formed by depositing a dielectric material over the entire surface of the wafer. Dielectric layer 14 may be formed using any material that is partially or wholly resistant to the conduction of electricity. Preferably, material used to form dielectric layer 14 also has a high dielectric constant. Such materials preferably include silicon oxides, silicon nitrides, silicon oxynitrides, tantalum oxide, barium strontium titanate, or the like. The particular thickness of dielectric layer 14 may depend on a particular application of capacitor 10, upon desired capacitor characteristics, and the like. However, in a particularly preferred embodiment of the present invention, dielectric layer 14 is approximately 50 to about 1000 Å thick.

With continued reference to Figure 5, a conductive material 42 is deposited over the surface of dielectric layer 14. In particularly preferred embodiments of the present invention, conductive material 42 includes films comprising: titanium nitride, titanium nitride/titanium/

titanium nitride, titanium nitride/tungsten, tantalum nitride/copper, combinations thereof and the like, with thicknesses ranging from about 800 to about 3000Å.

In accordance with a preferred embodiment of the present invention, top plate 16 formation includes patterning a substantially planar surface. Patterning over a substantially planar surface (*i.e.*, a surface that is substantially devoid of topography) allows substantially true pattern translation. For example, when a mask and photoresist are used to pattern the surface, translation of the defined pattern from the mask onto the wafer may be substantially true if the surface is substantially planar. Moreover, during subsequent capacitor top plate 16 formation, the photoresist pattern can be substantially accurately transferred to material 42 for substantially accurate definition of top plate 16, particularly if material 42 is sufficiently thin, for example, less than about 2000 Å. Sufficiently thin top plate 16 results in reduced localized etch profile variations, such as, for example, reactive ion etching lag, pattern dependent profile microloading, and the like, as well as reduced across-wafer material 14 film-thickness variations due to material 42 etch and over etch processes.

With reference now to Figure 6, top plate 16 of capacitor 10 may be formed over dielectric layer 14 in a variety of ways. Preferably, top plate 16 is formed by coating material 42 with photoresist, patterning the photoresist, developing the photoresist, and etching material 42 to form top plate 16. In accordance with preferred embodiments of the present invention, dielectric material 14 acts as an etch stop layer for material 42 etch such that material 42 etchants do not react with material 18 and the like.

With reference now to Figures 7 and 8, a spacer 48 may be formed about the perimeter of top plate 16 to, among other things, protect the perimeter interface between dielectric 14 and top plate 16 from potential chemical attack or degradation during subsequent wafer processing. Spacers 48 are preferably configured to minimize potential interaction between capacitor 10 materials and other materials on the wafer surface to reduce defect density at the perimeter of capacitor 10 and improve capacitor 10 reliability.

Spacer 48 is preferably formed by depositing an insulating material 44 onto the wafer surface. Material 44 may include silicon oxide, silicon nitride, and/or the same material as dielectric 14, which may be deposited using chemical vapor deposition, spin-on techniques, and the like. Preferably, about 500 to about 3000 Å of material 44

is deposited onto the wafer surface; the thickness of the material 44 is preferably greater than or equal to the thickness of the dielectric 14. Spacers 48 may be defined by removing material 44 from all parts of the wafer except near sidewalls 46 of plate 12.

Any number of conducting, semi-conducting, semi-insulating or insulating films may be added to the surface of the wafer after capacitor 10 is formed. For example, as shown in Figure 1, insulating layer 20 may be deposited onto the surface and subsequently planarized using CMP. Conductive plugs 50 and lines 52 may be formed in accordance with the damascene methods described above. Preferably, the etchant used during damascene processing to remove material 20 etches material 20 at a rate greater than it etches plate 16 material, so that the etch does not punch through top plate 16 and attack dielectric 14, or to base plate 12 to create unwanted capacitor shorts. The surface of layer 20 may then be planarized to form the structure shown in Figure 1.

In accordance with a preferred embodiment of the present invention, methods for forming capacitors 10 and the like are preferably chosen such that, if possible, minimal additional or new process steps are required to form the capacitors. Accordingly, the process flow sequence described for the forming the structure shown in Figure 1, including capacitor 10, preferably requires only a single additional patterning step in addition to typical damascene interconnect processes. The addition of only one additional masking step makes the addition of capacitor 10 relatively simple and inexpensive.

In accordance with an alternate embodiment of the present invention and as shown in Figure 9, a capacitor 100 may suitably be formed without the inclusion of spacers. Capacitor 100 may be advantageous because it requires fewer processing steps to form the device. However, capacitor 100 may be susceptible to potential chemical attach and resulting degradation due to, for example, subsequent processing steps.

In accordance with an alternate embodiment of the present invention and as shown in Figure 10, top plate 202 of capacitor 200 may be larger in area than base plate 204. In this case, an electrical connection to base plate 204 may be formed using the methods noted above, specifically, damascene and/or dual damascene

processes. The "positive overhang" of top plate 16 allows additional conductive plugs 206 to be positioned in the overhang region. In accordance with various aspects of this embodiment, plugs 206 above top plate 202 may be positioned substantially in a region defined by the overhang. If top plate 202 "overhangs" base plate 204, capacitor 200 formation may be less sensitive to etchants used to form vias and the like in insulating material 208.

Referring now to Figure 11, in accordance with another embodiment of the present invention, a capacitor 300 may be formed in the top most metallization layers on the wafer surface. Forming capacitor 300 on the upper most layers may be advantageous because, among other reasons, parasitic capacitance between capacitor 300 and the substrate is reduced. Consequently, this embodiment may be particularly desirable in high frequency (*e.g.*, RF) applications where parasitic capacitance is particularly problematic. Capacitor 300 formation may require additional masking and etching strips to form capacitor dielectric layer 302. Layer 302 is preferably patterned and etched prior to top plate 304 formation such that electrical connections may be made to structure features beneath layer 302.

Referring now to Figure 12, a capacitor 400 with a top plate 402 offset from a bottom plate 404, in accordance with an alternate embodiment of the present invention, is shown. Offsetting top plate 402 allows for electrical connections to both top plate 402 and base plate 404 to be formed from either a top or bottom surface of capacitor 400.

In accordance with yet another embodiment of the present invention, a capacitor 500 including various metal features such as lines 502, formed during process step separate and distinct from process steps used to form plates 504 and 506, is shown in the structure illustrated in Figures 13 and 14. This process typically requires additional masking and etching steps to form features 502. In accordance with preferred aspects of this embodiment, dielectric layer 508 preferably overhangs base plate 506.

In alternate embodiments of the present invention, etch stop layers may be used to define a surface of a plate of the capacitor, an opening for a via, or combinations thereof. In addition, various capacitor plate configurations may be formed to allow

electrical connections between the capacitor plates and other devices integral with or external to the semiconductor wafer.

With reference to Figure 15, a thin-film capacitor 600 in accordance with an alternate embodiment of the present invention may be formed using a dual damascene process. Capacitor 600 preferably includes a bottom plate 602, a top plate 604 and an insulating layer 606 interposed therebetween. Other structures may be formed on the surface of the wafer during capacitor 600 fabrication. These structures may include, for example, feature 608, which may include metal lines and the like. Other features or devices such as resistors may also be simultaneously formed on the surface of a wafer during capacitor 600 formation.

With reference to Figure 16, capacitor 600 may be formed on a surface of a semiconductor wafer by first depositing an insulating material 610 over the surface of a wafer. A hard mask material 612, such as for example silicon nitride or any other material that is resistant to particular etchants that may be used to etch insulating layer 610, may then be deposited. Hard mask material 612 is preferably used to define a bottom surface of bottom plate 602 of capacitor 600. Also, hard mask material 612 may be used to define an aperture 614, which allow etchants to dissolve or vaporize insulating material 610 or other layers beneath hard mask material 612. In preferred embodiments of the present invention, hard mask material 612 may comprise silicon nitride, and aperture 614 may be formed by etching material 612 with any suitable etchant, for example a fluorine-based etchant such as SF_6.

Referring now to Figures 17 and 18, bottom plate 602 of capacitor 600 is preferably formed within an insulating material 616. Accordingly, bottom plate 602 is formed by depositing insulating material 616 over the surface of the wafer and etching material 616 to form openings 618, 620, using, for example, methods described above. In preferred embodiments of the present invention, insulating material 616 is planarized using CMP prior to patterning and etching fabrication steps. The etch used to form opening 618, 620 is preferably selective, such that it etches insulating material 616 at a much higher rate than it etches hard mask material 612. For example, insulating material 616 may include silicon oxide or a doped silicon oxide material and hard mask 612 may include silicon nitride. In such a case, a typical dry etch process

may include etching insulating material with a fluorine-based etchant such as CHF_3 or SF_6.

The bottom of opening 618 is preferably defined by the top surface of hard mask material 612. Similarly, a portion of opening 620 has its bottom surface defined by hard mask 612. Aperture 614 in hard mask material 612 facilitates etching of a portion of insulating material 610 to form via 622 during a process step that also involves etching insulating material 616. Preferably, via 622 extends to a conductive feature 624 underneath insulating material 610.

Bottom plate 602 of capacitor 600 and various other features such as feature 608 and a conductive plug 626 may be formed by depositing a conductive material and removing a portion of the conductive material as described above.

With reference now to Figure 19, insulating layer 606 may be formed by depositing insulating material over the surface of a wafer. The insulating material may include any of the capacitor dielectric materials described above.

Referring now to Figure 20, top plate 604 of capacitor 600 may be formed using film deposition, pattern, and etch processes described above. After top plate 604 formation, any number of additional layers may be deposited onto and patterned on the wafer surface. For example, as shown in Figure 15, insulating layer 628 and conductive feature 630 may be formed on the wafer surface.

The terms top and bottom have been used throughout this application to refer to various layers, plates and surfaces. These terms are used for reference to the drawing figures only and are not meant to limit possible configuration of capacitors described hereinabove. In addition, although the present invention is set forth herein in the context of the appended drawing figures, it should be appreciated that the invention is not limited to the specific forms shown. Various other modifications, variations and enhancements in the design and arrangement of the thin-film capacitors as set forth herein may be made without departing from the spirit and scope of the present invention as set forth in the appended claims. For example, various feature or devices such as conductive lines, resistors, and the like may be formed on a surface of a wafer during capacitor formation.

CLAIMS

What is claimed is:

1. A method for forming a capacitor on a surface of a substrate, the method comprising the steps of:

depositing a first insulating material on the surface of the substrate;

forming a trench within said insulating material;

depositing a first conductive material onto said first insulating material;

removing a portion of said conductive material such that the top surface of said first conductive and said first insulating material are substantially planar;

forming an insulating layer over said conductive material; and

forming a top plate of a capacitor, wherein said top plate is formed by depositing a second conductive material and etching said second conductive material such that at least a portion of said second conductive material resides over said insulating layer and substantially above said first conductive material.

2. The method for forming a capacitor on a surface of a substrate of claim 1, the method further comprising the step of forming a via within said second insulating material.

3. The method for forming a capacitor on a surface of a substrate of claim 2, the method further comprising the step of forming a conductive plug within said via.

4. The method for forming a capacitor on a surface of a substrate of claim 1, the method further comprising the step of forming an electrical connection between a top surface of the wafer and said bottom plate.

5. The method for forming a capacitor on a surface of a substrate of claim 1, the method further comprising the step of forming an electrical contact to said top plate of said capacitor.

6. The method for forming a capacitor on a surface of claim 1 further comprising the step of forming a spacer about a perimeter of said top plate.

7. The method of claim 1 further comprising forming an etch stop layer, wherein said etch stop layer defines a surface of said base plate.

8. A thin-film capacitor formed on a surface of a substrate, the capacitor comprising:

a first insulating layer having a bottom plate of a capacitor and a conductive feature formed therein;

a second insulating material having a top plate of the capacitor and a conductive feature formed therein, wherein said conductive feature is in electrical contact with said base plate; and

a dielectric material interposed between said first and second insulating layers, wherein said dielectric material is also interposed between said bottom and top plates.

9. The capacitor of claim 8 further comprising a spacer about a perimeter of said top plate.

10. The capacitor of claim 8 further comprising a spacer about a portion of said dielectric material.

11. The capacitor of claim 8, wherein said top plate is larger than said base plate.

12. The capacitor of claim 8, wherein said base plate is larger than said top plate.

13. The capacitor of claim 8, wherein said top plate overhangs a portion of said base plate.

14. The capacitor of claim 8 wherein said dielectric material comprises barium strontium tantinate.

15. The capacitor of claim 8 wherein the dielectric thickness is about 50 angstroms to about 1000 angstroms.

16. The capacitor of claim 8 wherein said bottom plate material comprises titanium, titanium nitride and aluminum copper.

17. The capacitor of claim 16 wherein the thickness of said base plate is about 1000 angstroms to about 1 micron thick.

18. The capacitor of claim 8 wherein said top plate material comprises titanium nitride.

19. The capacitor of claim 8 wherein the thickness of said top plate is about 800 angstroms to about 3000 angstroms thick.

20. A thin-film capacitor formed on a surface of a substrate, the capacitor comprising:

a base plate formed within a first insulating material;

a dielectric layer over said base plate and a portion of said insulating material; and

a top plate formed within a second insulating material, wherein said top plate is formed by depositing a conductive material and etching a portion of said conductive material.

21. The capacitor of claim 20 wherein said top plate overhangs at least a portion of said base plate.

22. The capacitor of claim 20 wherein said base plate is larger than said top plate.

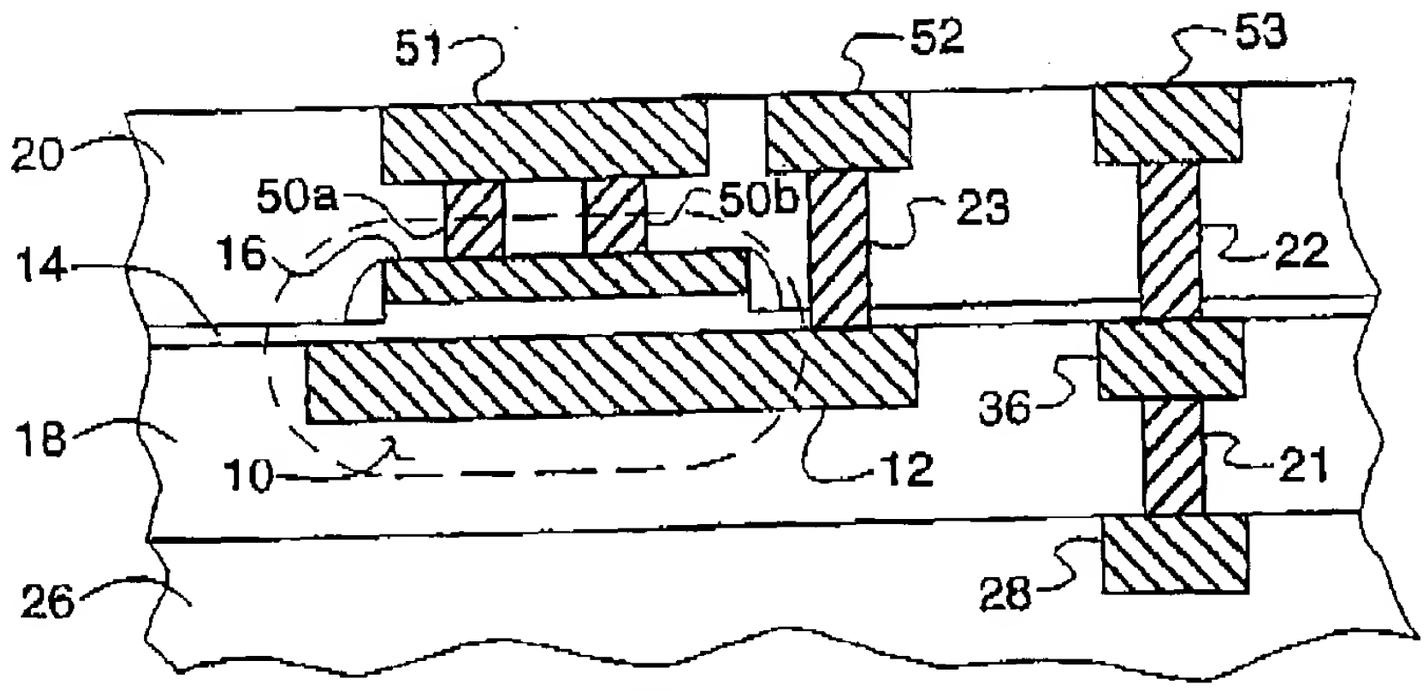


FIG. 1.

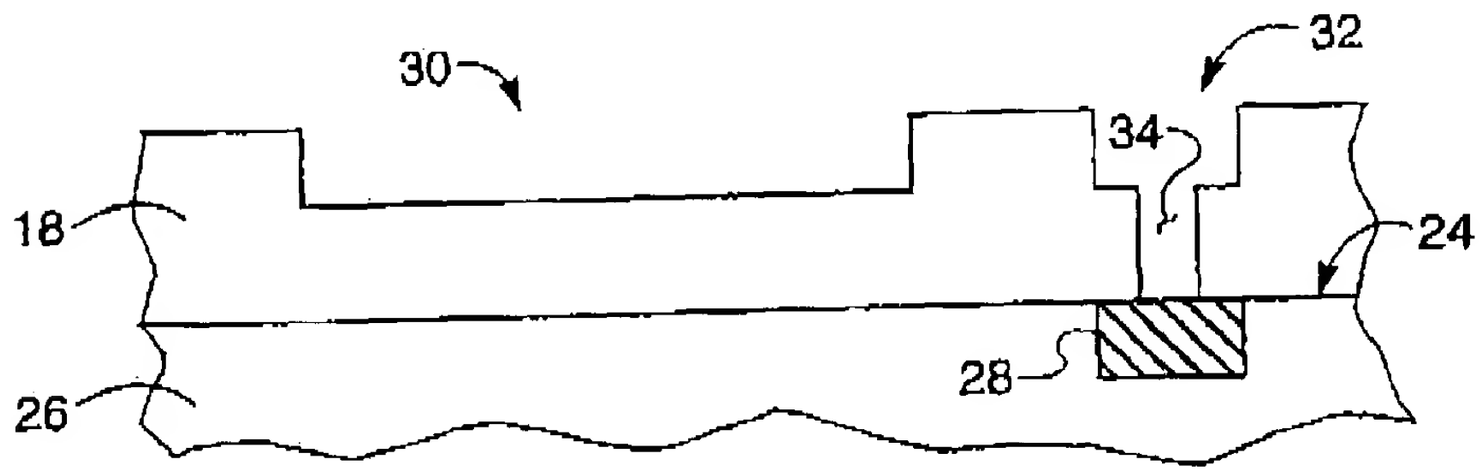


FIG. 2.

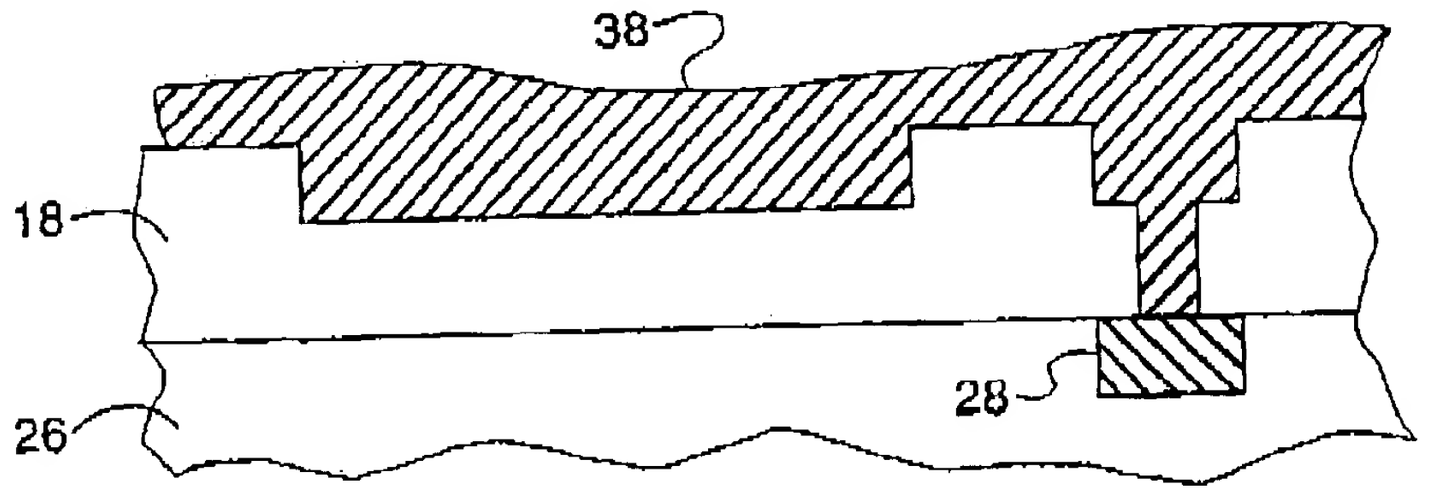


FIG. 3.

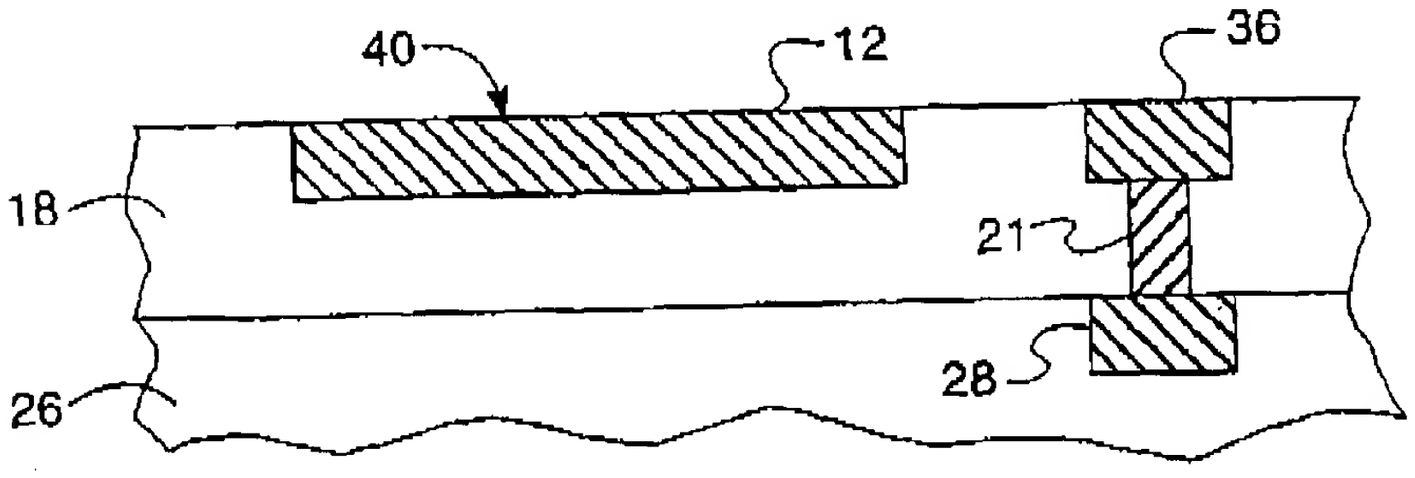


FIG. 4.

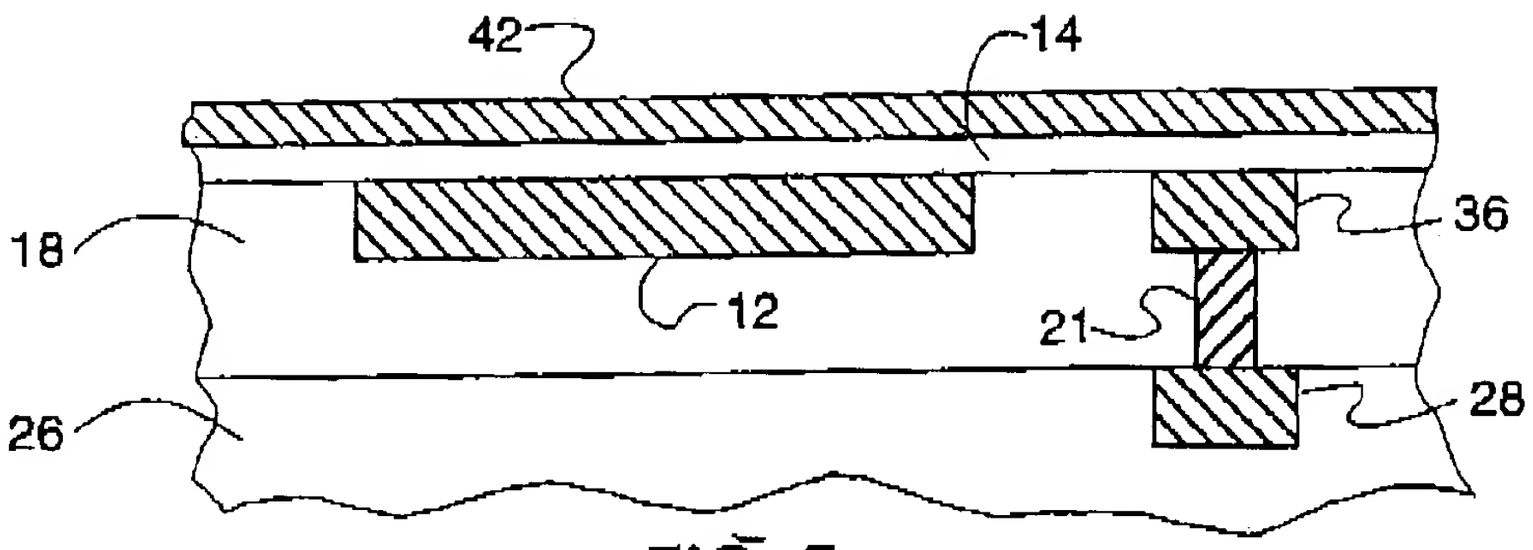


FIG. 5.

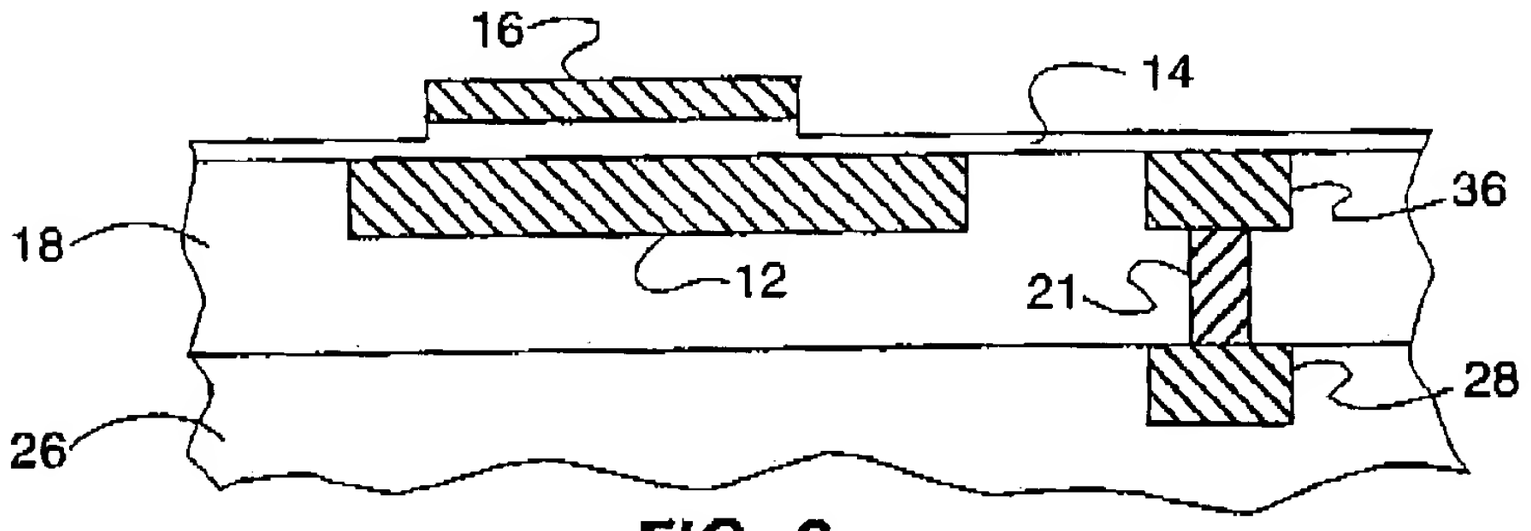
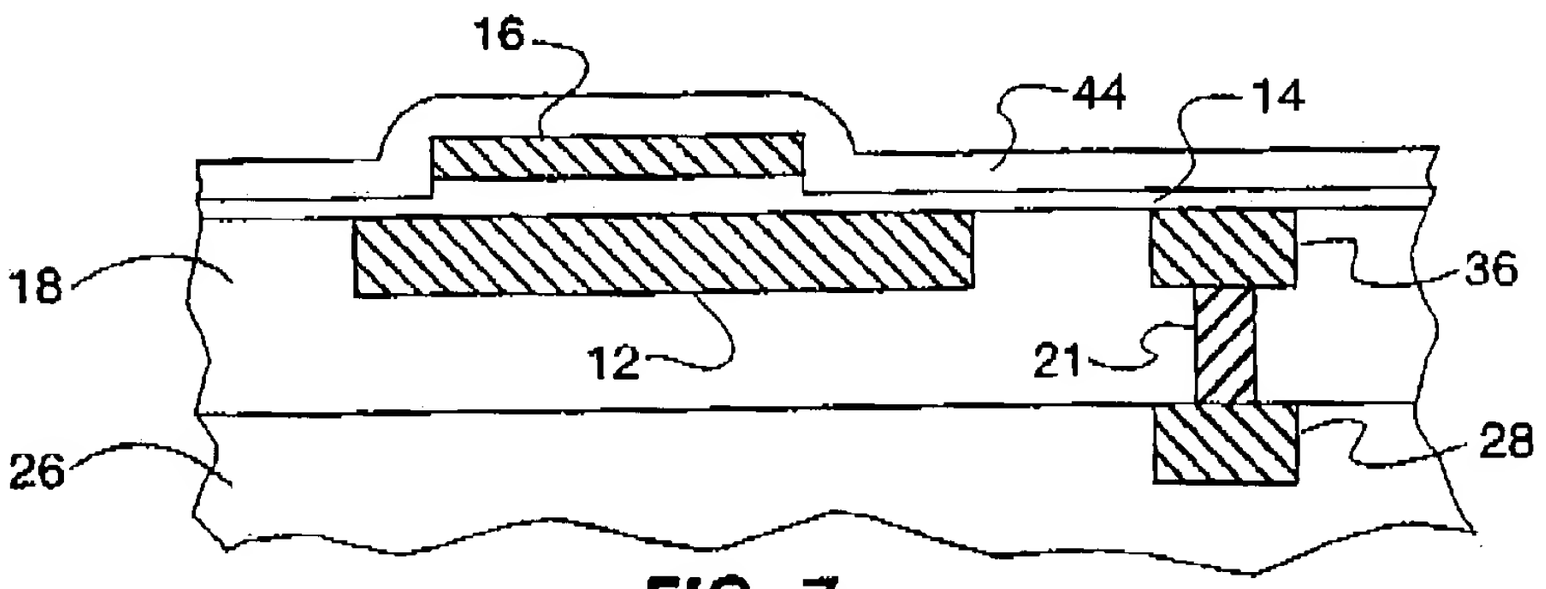


FIG. 6.



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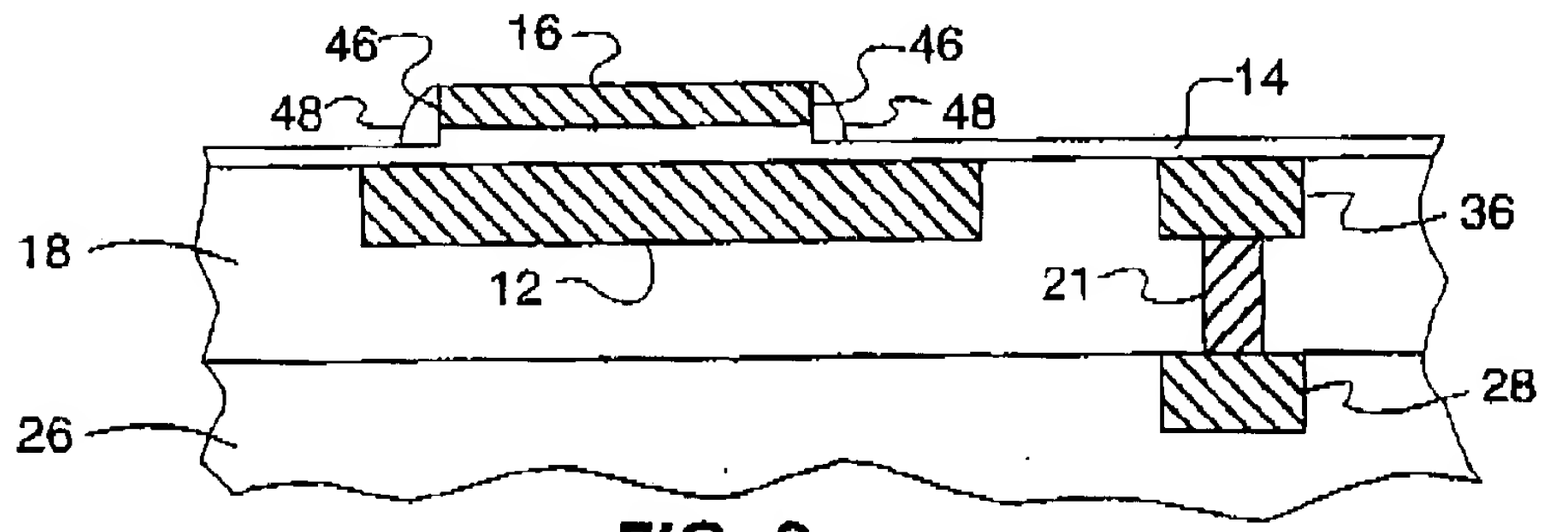
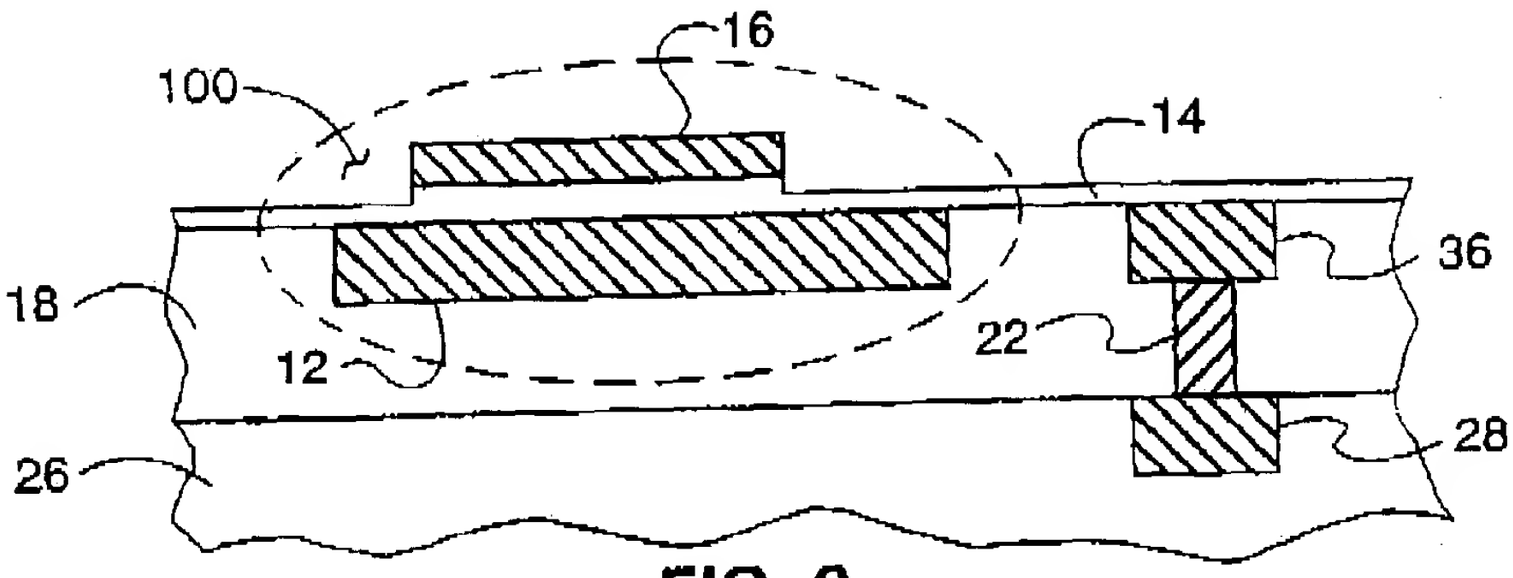


FIG. 8.



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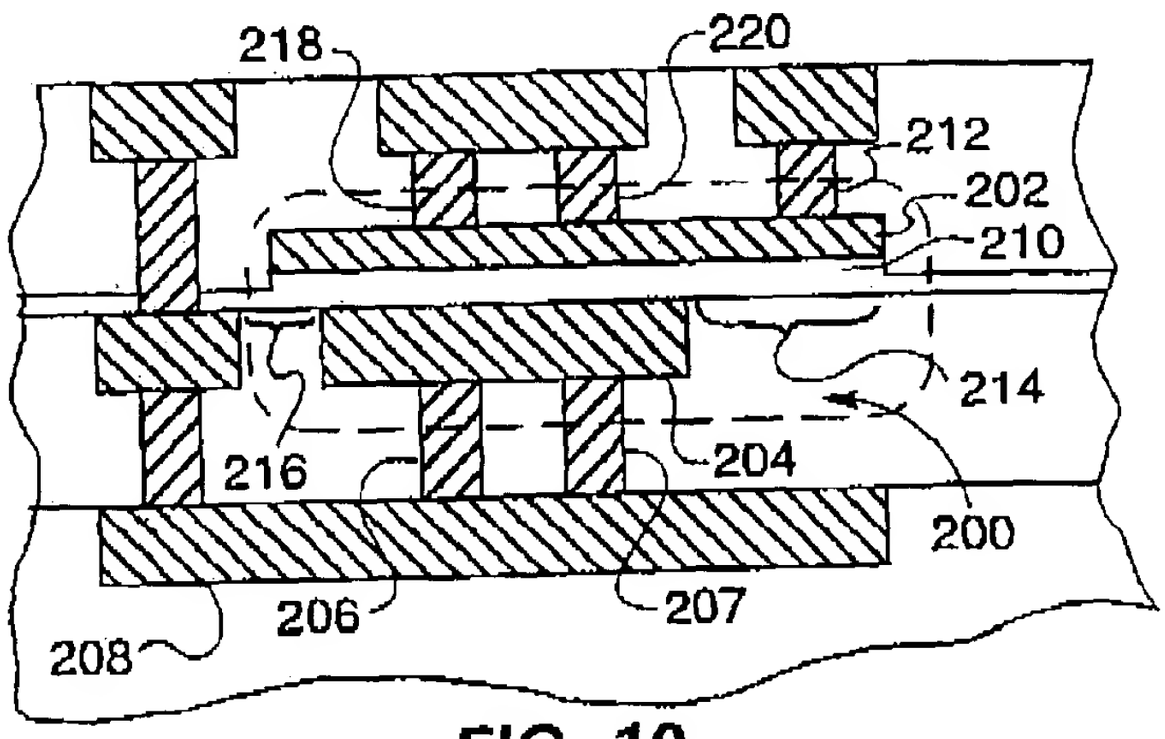
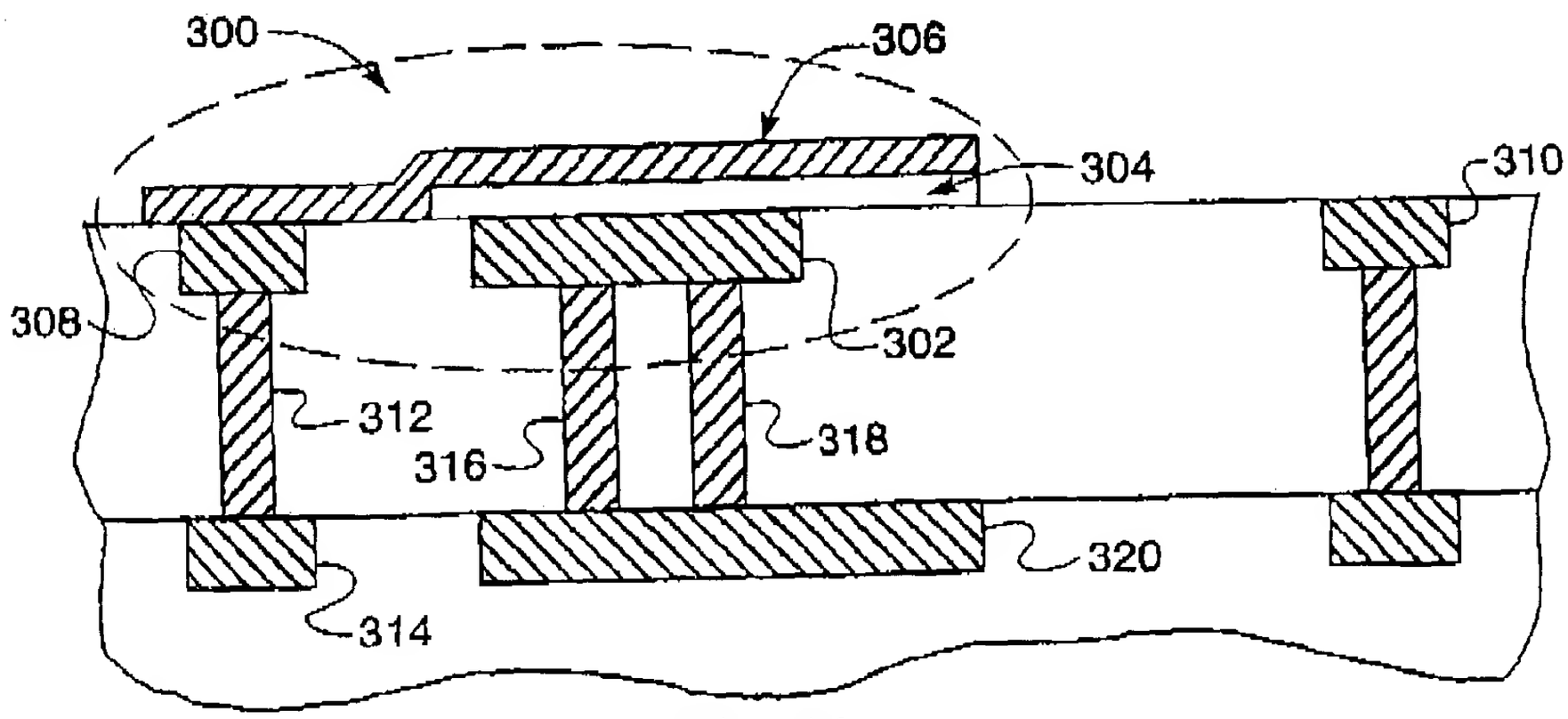


FIG. 10.



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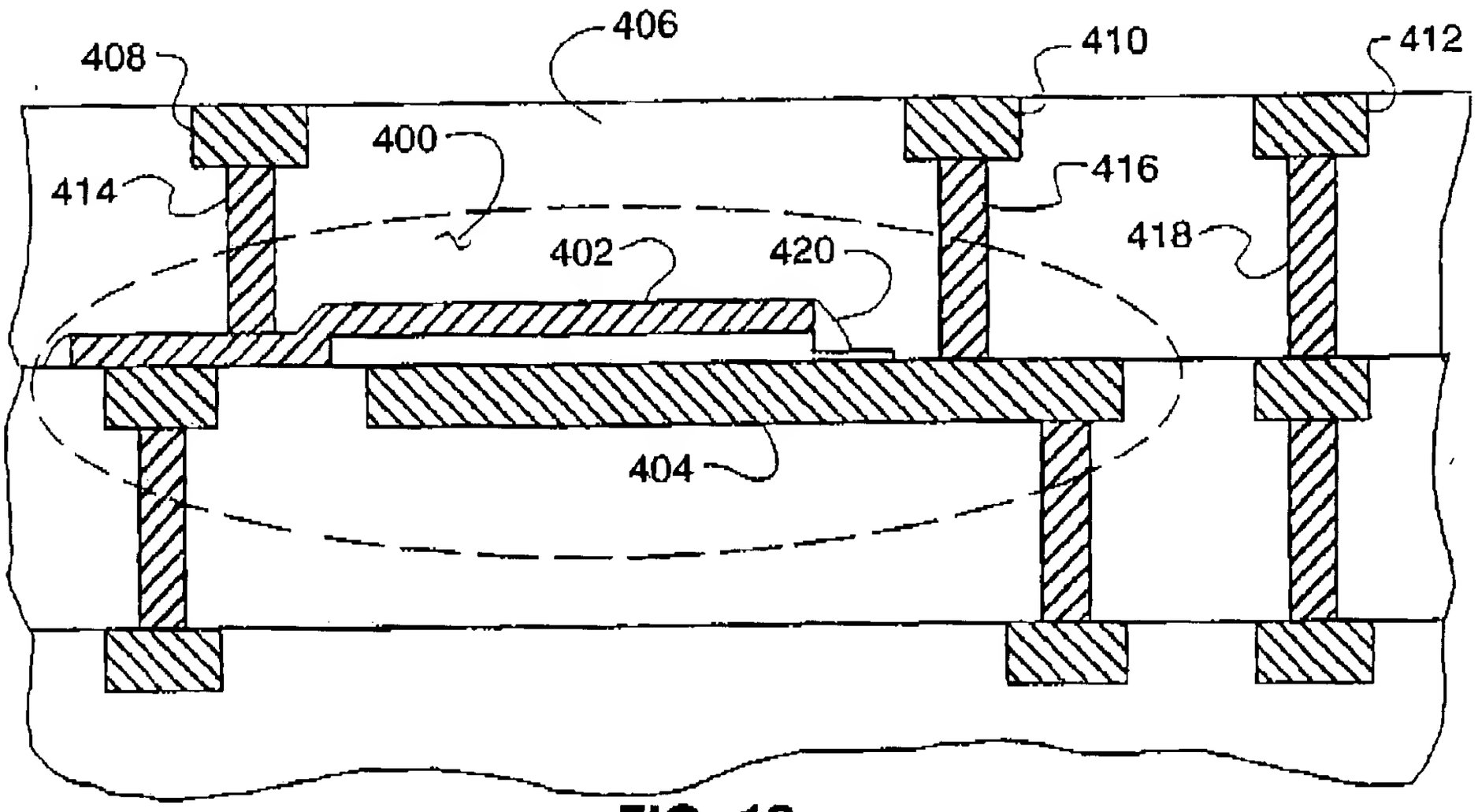

FIG. 12.

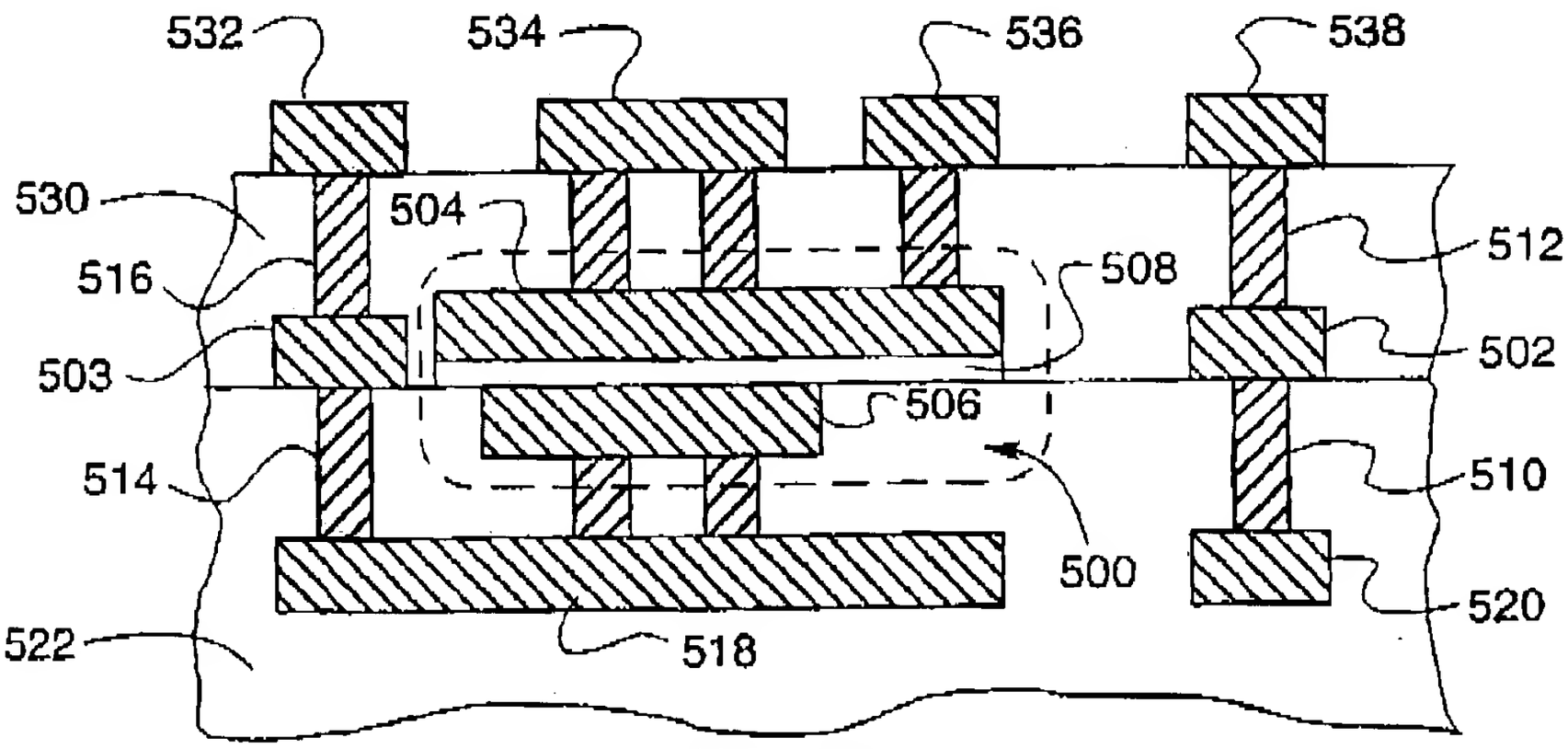

FIG. 13.

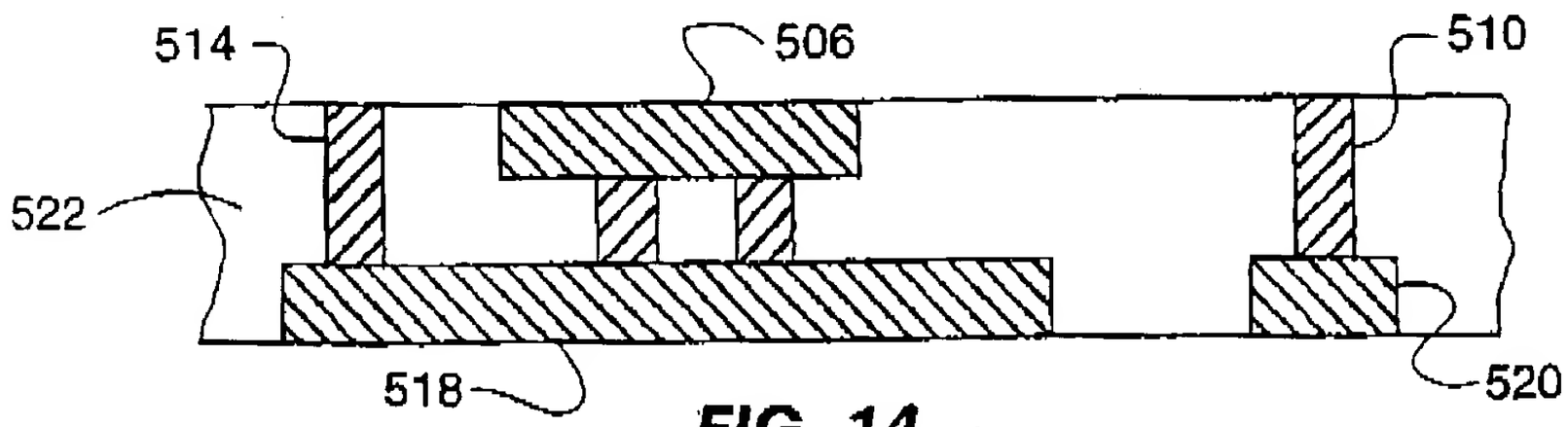

FIG. 14.

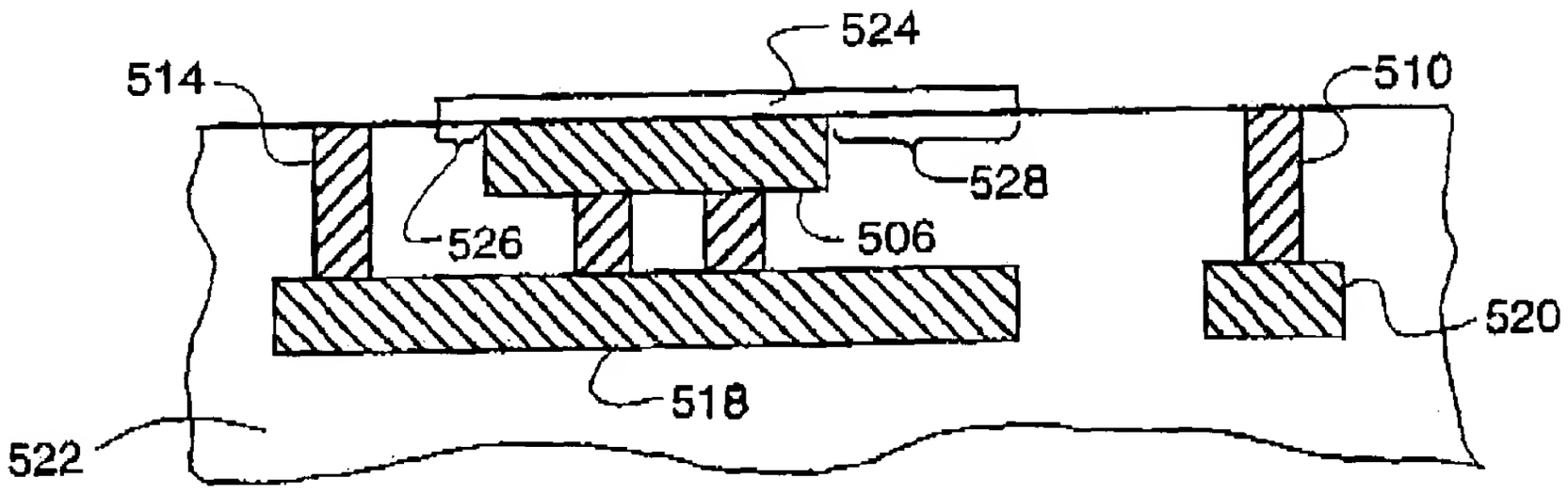

FIG. 15.

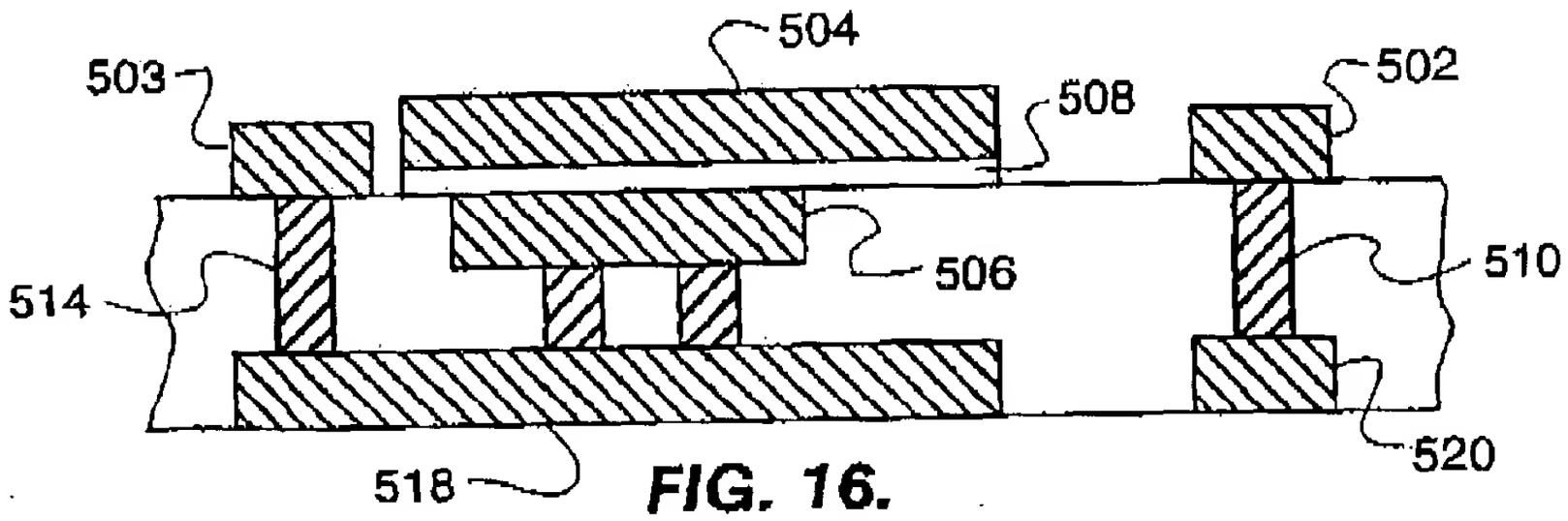

FIG. 16.

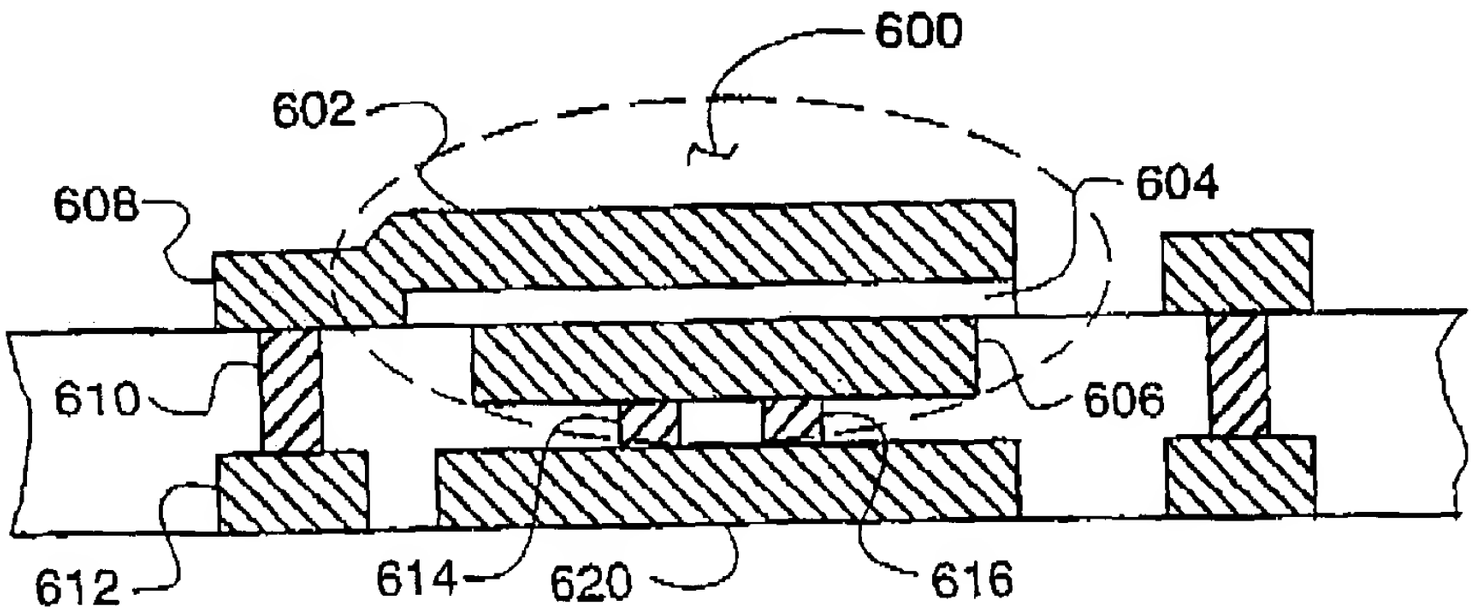

FIG. 17.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/02760

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 808 855 A (TEO YEOW MENG ET AL) 15 September 1998 (1998-09-15) column 5, line 44 -column 12, line 9; figures 2A-2F	1,8,20
P,X	EP 0 975 018 A (STMICROELECTRONICS SA ;FRANCE TELECOM (FR); KONINKL PHILIPS ELECTR) 26 January 2000 (2000-01-26) figures 1-4	8,20
A	EP 0 800 217 A (IBM) 8 October 1997 (1997-10-08) abstract; figure 1	1,8,20
A	EP 0 771 022 A (IBM) 2 May 1997 (1997-05-02) cited in the application the whole document	1,8,20

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 July 2000	13/07/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Königstein, C

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/02760

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		SG 45510 A	16-01-1998
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